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TAIWAN INNOVATION CONFERENCE

Noise Coupling Analysis For Share Power Source System

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Agenda

- Introduction to PHISON.
- Possible Problem in Share Power Source System.
- How to Analyze It?
- Possible Solution.
- Conclusion

Introduction to PHISON

Experience

20+ Years

3 Priorities

Consumer | Embedded | Enterprise

2100+ HC

70% R&D

600M

Average annual controller shipments

1900+

Worldwide patents

$1.45B

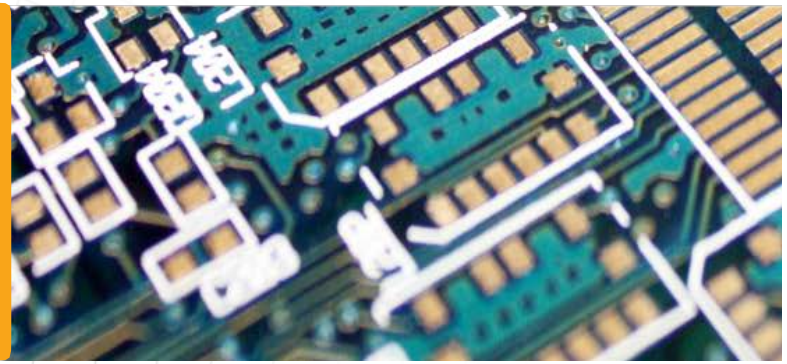
2019 Revenue, no debt

Introduction to PHISON

Introduction to PHISON

NAND Flash-based IC Design

Over 20 years of expertise developing NAND flash controllers
- 1900+ flash related patents[1], Internal Phy, ASIC, and advanced NAND handling technologies



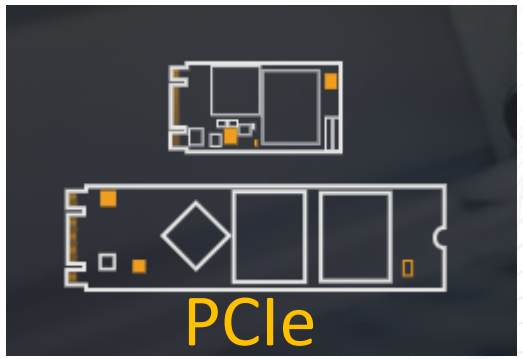
System Integration

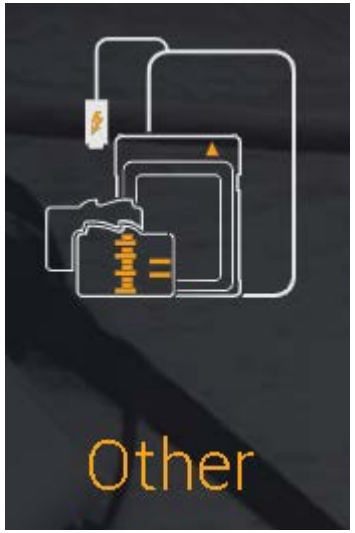
Extensive expertise in mainstream applications
- Embedded, Enterprise, PC, and Mobile
- PATA, SATA, PCIe NVMe, USB, SD, eMMC, UFS

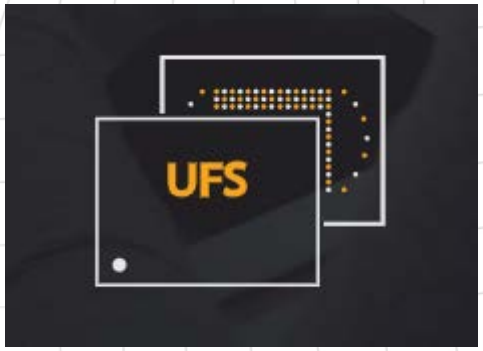
ODM | From Design to Manufacturing

Turnkey | Flexible Business Model

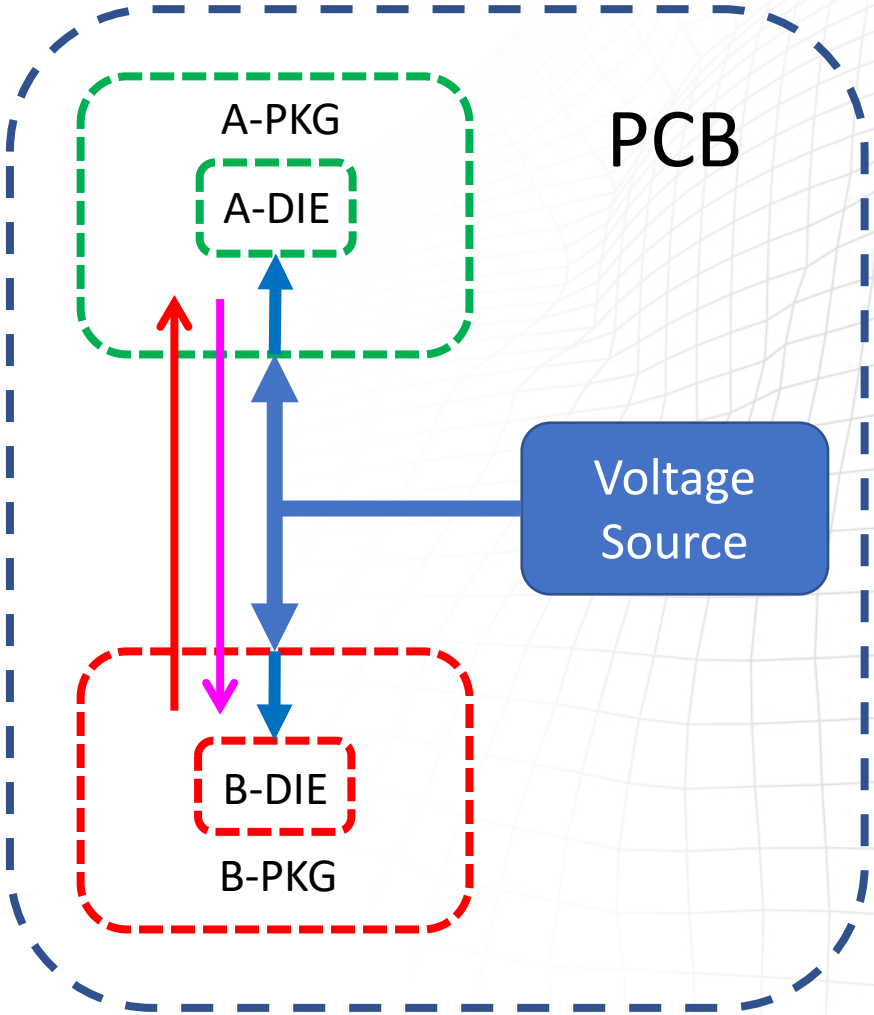
Introduction to PHISON







Possible Problem in Share Power Source System

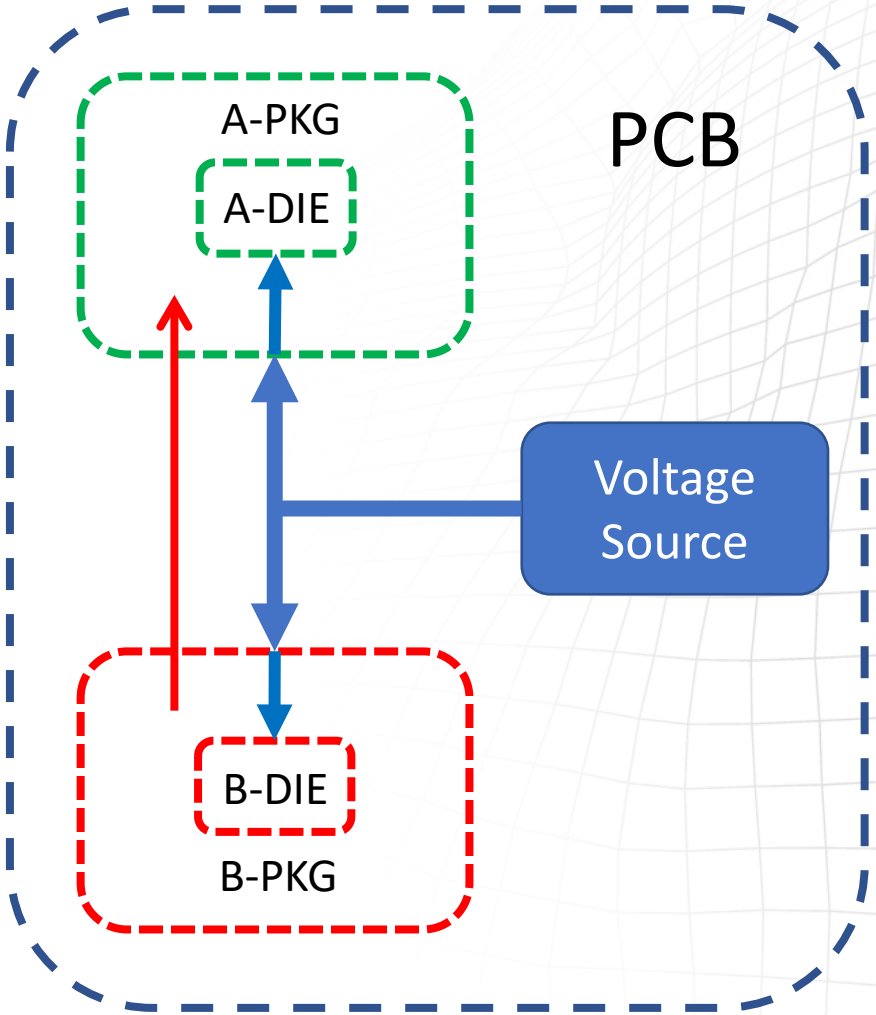


Voltage noise from B to A

Voltage noise from A to B

- Power rail A and B are same voltage.
- Total noise at A = noise generated by A + noise from B.
- Total noise at B = noise generate by B + noise from A.

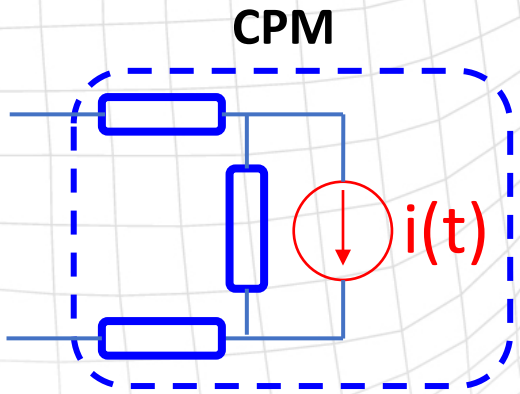
How to Analyze It? (1/4)



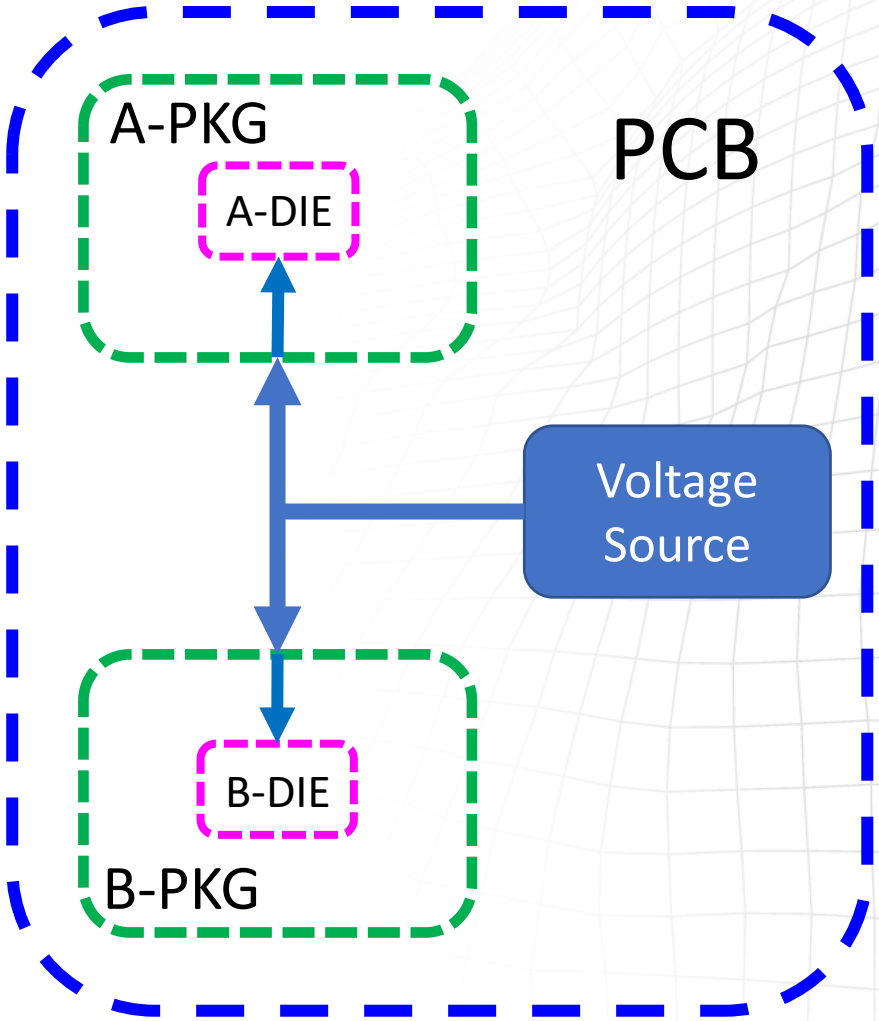
- Total noise at A = noise generated by A + noise from B
- Noise generate by A => CPM (Chip Power Model)
- Noise generate by B => CPM
- Noise Path => PKG/PCB model

noise generated by A => related to Z(f)

noise form B => related to S21



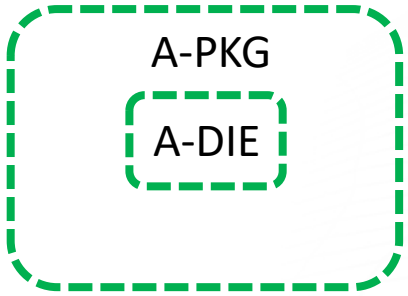
How to Analyze It? (2/4)

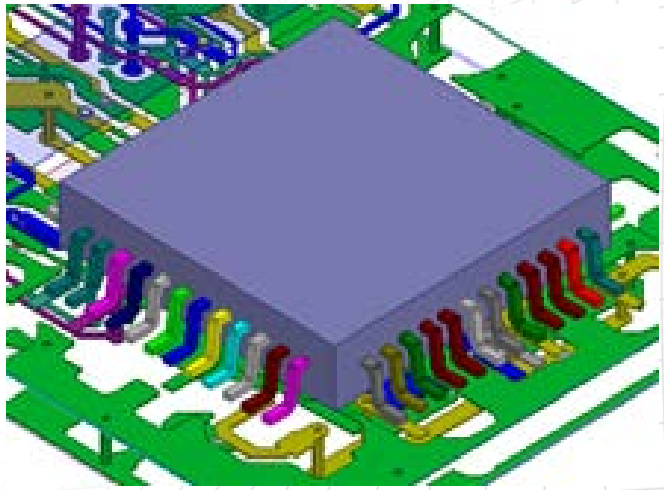


Tools

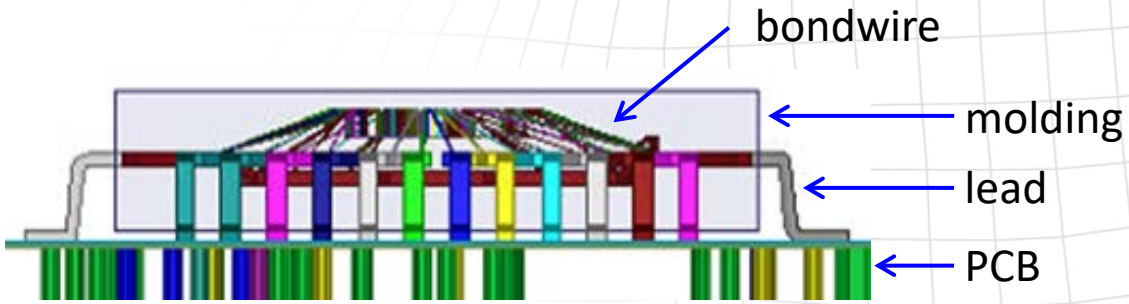
- A/B-DIE => CPM (Chip Power Model) => RedHawk/Totem
- A/B-PKG model => HFSS/SIwave/Q3D
- PCB model => HFSS/SIwave

How to Analyze It? (3/4)

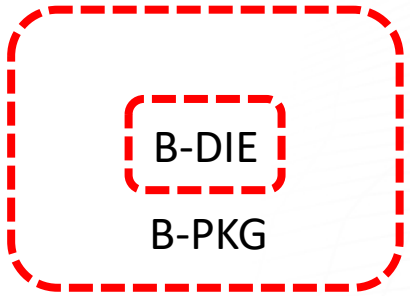


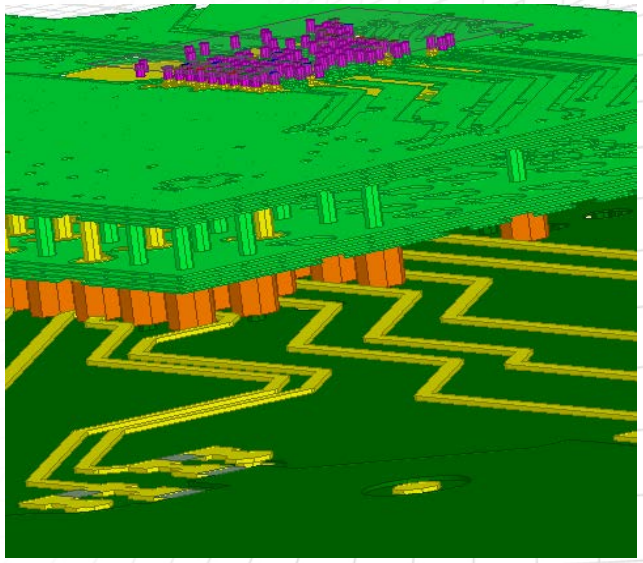


- A-PKG is QFP
- Import QFP 3D file (.sat/.stp)
- Include bondwire
- Import PCB layout file (.brd)
- Merge PKG and PCB, co-extraction by HFSS

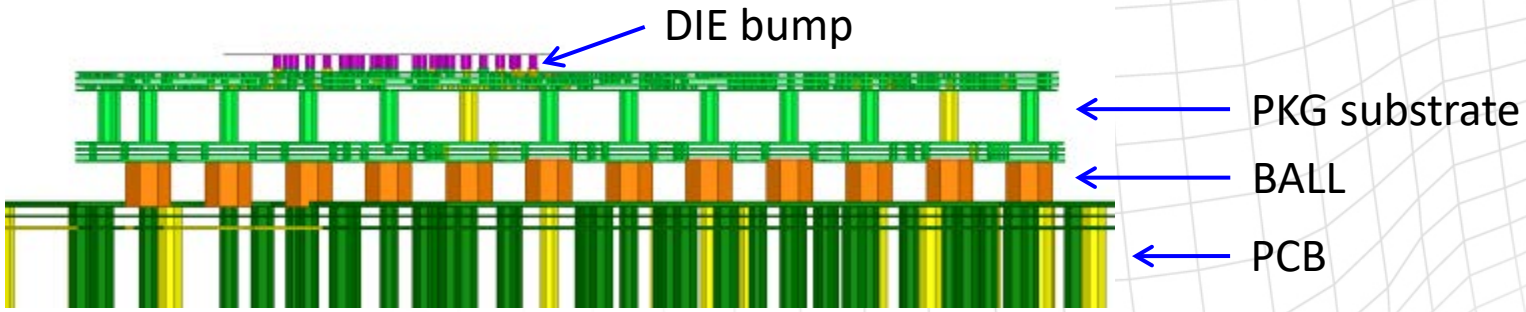


How to Analyze It? (4/4)

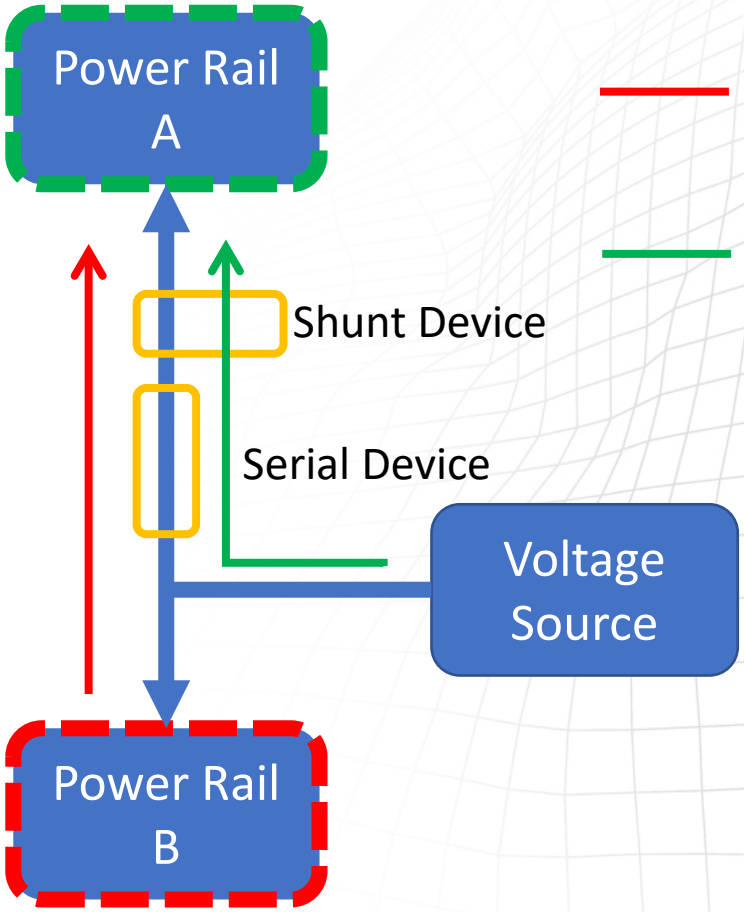




- B-PKG is Flip-Chip BGA
- Import PKG layout file (.mcm)
- Include bump
- Import PCB layout file (.brd)
- Merge PKG and PCB, co-extraction by HFSS



Possible Solution(1/3)



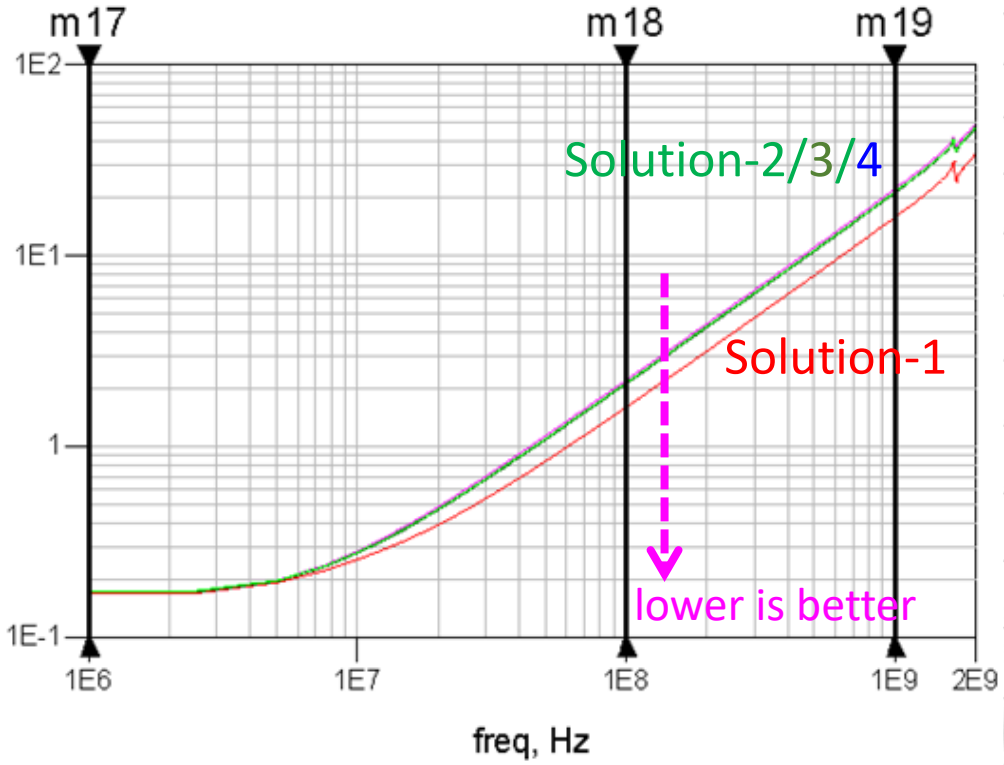
Noise path
Block; check by (S21)

Original power path
Lower; check by Z(f)

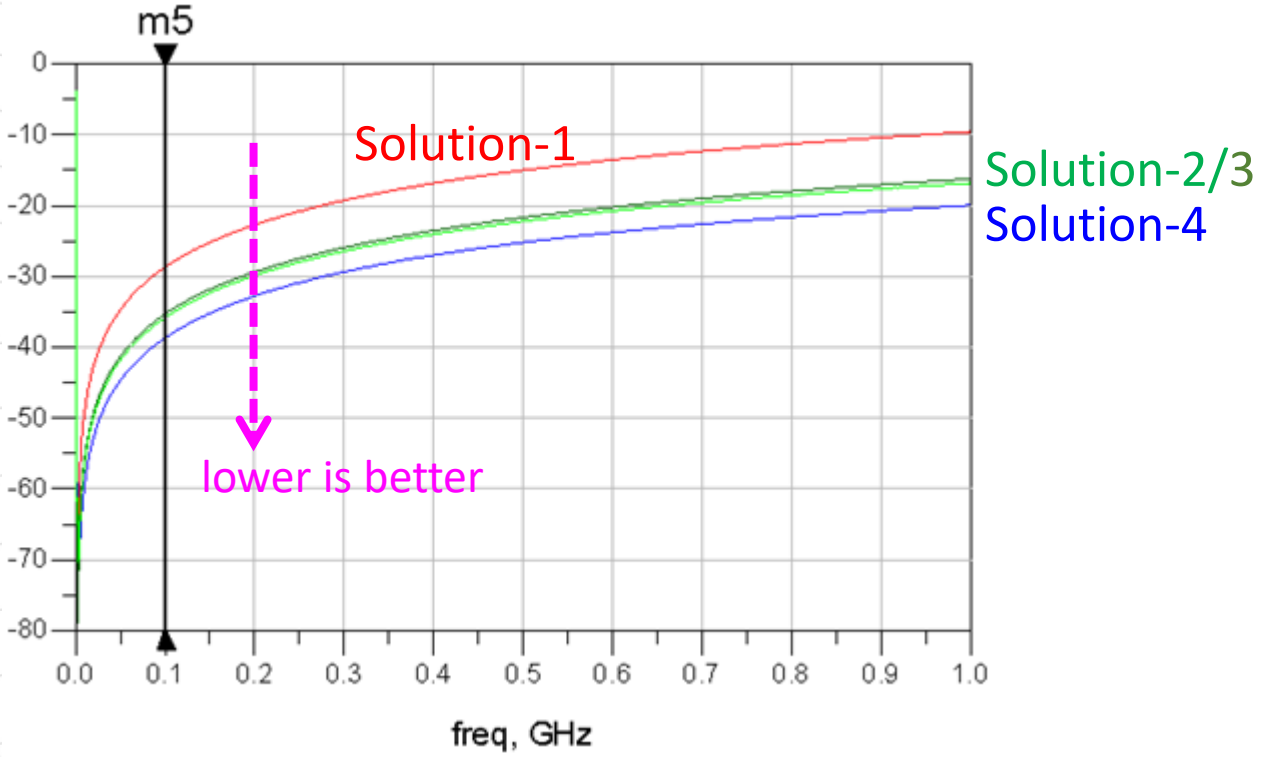
- Serial Device => inductor, ferrite bead
- Shunt Device => capacitor
- Device Placement
- Routing Topology
- Check both Z(f) and S21 (trade-off)

Possible Solution(2/3)

Z(f) from A DIE PAD

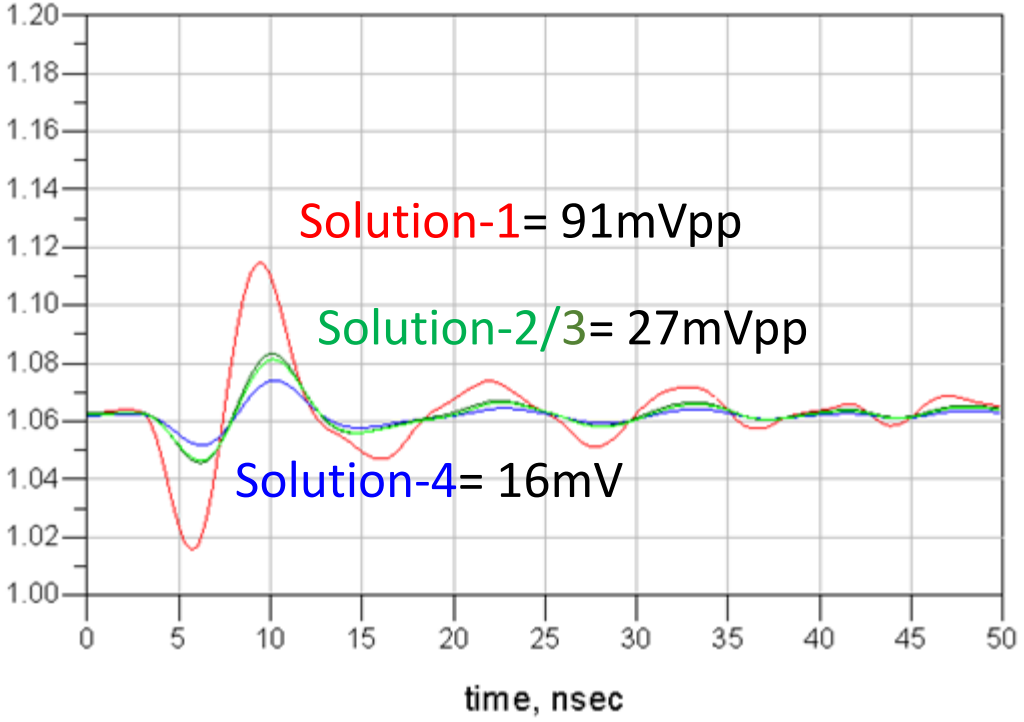


S21 between A/B DIE PAD

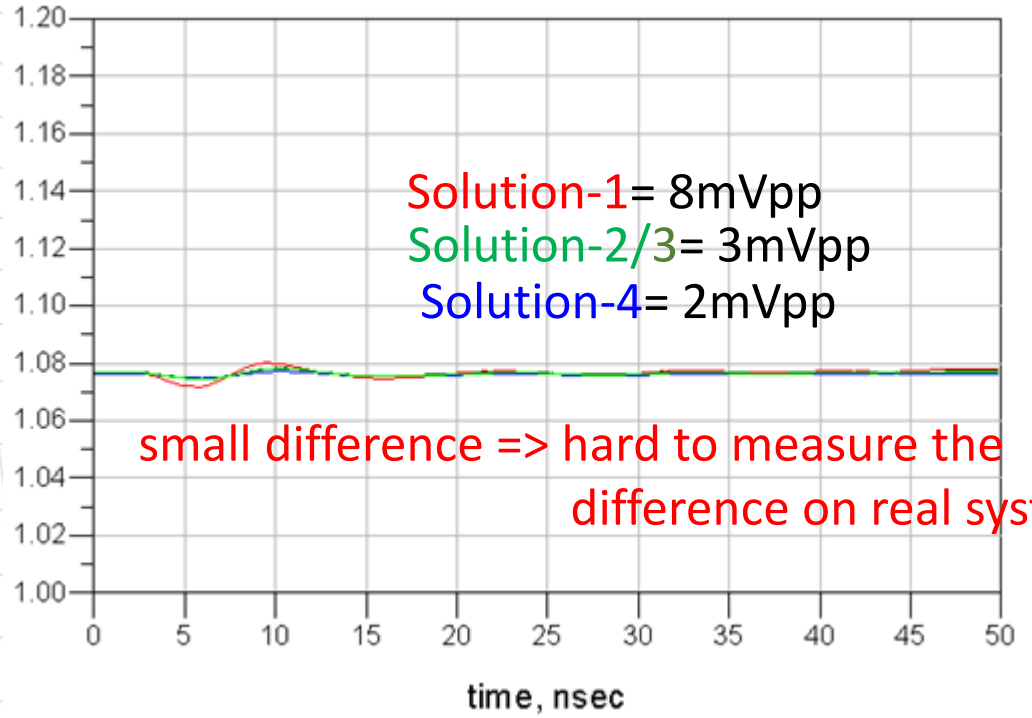


Possible Solution(3/3)

Voltage noise from B; probe at A DIE PAD



Voltage noise from B; probe at shunt device



small difference => hard to measure the difference on real system.

Conclusion

- We need consider both Z(f) and S21 for share power source system.
- We need use more than one tool for system level PI simulation.

  RedHawk/Totem/HFSS/SIwave/Q3D in this case.
- Voltage fluctuation is large at DIE PAD, but small at external shunt device.

  The role of simulation is important, because it is hard to measure the small difference on external shunt device.

問題一 共用電源時的設計, 要注意什麼?

一般我們都只會檢查chip-A或chip-B本身造成的noise
也就是看power path的Z參數
如果是共用電源的設計, chip-A跟chip-B會透過PCB的路徑, 互相干擾
這時候我們可以透過檢查S21參數來評估
更進一步的話, 可以模擬出voltage noise來評估

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問題二 為什麼要用到CPM(chip power model)

CPM像是個激發源
他描述了DIE的i(t)及DIE的parasitic
如果只有PKG或PCB model, 這樣只能看到S參數
看不到最後的voltage noise
結合CPM與PKG/PCB model, 可以看到最終的voltage noise

問題三 在這個case中, 你覺得simulation比起量測的優勢在哪裡?

在這個case中, 我們try了4種solution
實際待測物在功能測試時, 是會有不同的改善程度
但是在chip外部量測時, voltage noise幾乎沒有差異
透過simulation我們可以看到, 4種solution在DIE端的voltage noise差異是大的
趨勢也跟功能測試相符合
代表simulation可以分析量測難以達到的地方

問題四 在這個case中, 最難的部分是什麼?

以往我們會把PKG跟PCB分開抽取參數
由於這個case的noise是從PKG-B透過PCB傳到PKG-A
為了更準確, 我們是把2個PKG跟PCB merge在一起抽參數
另外也把bondwire及bump結構也建到model中